REMARKS

Claims 17-23, 25 and 46-59 are pending in the present application.

The parent patent application, serial no. 08/159,461, was filed with claims 1-55, which were subject to a restriction requirement.

Claims 1-16, 24 and 26-45 were canceled as directed to a species elected in the parent application.

Claims 17 and 25, which previously depended from canceled claims, were amended to place the claims in independent form. The scope of those claims was not altered by the amendments.

Claims 18, 20-23 and 50-52 were amended to correct typographical errors and to improve the clarity of the claims by eliminating superfluous terms and using terms consistently. The scope of those claims was not altered by the amendments.

Claims 56-59 have been added.

Examination of the application on the merits is respectfully requested.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claims 17-18, 20-23, 25 and 50-52 were amended herein as follows:

17. (amended) [The]A method of [claim 1, wherein said forming step comprises]fabricating a portion of a semiconductor device comprising:

forming a gate structure on a substrate by:

depositing [the]an insulating oxide layer on the substrate;

depositing [the]a nitride layer on the oxide layer; and

depositing [the]a polysilicon layer on the nitride layer; and

reoxidizing the gate structure to form a layer of oxide over the gate structure.

18. (amended) The method of claim 17, wherein the depositing step includes depositing the nitride layer on the insulating oxide layer to a thickness from about 10 Å to about 50 Å.

20. (amended) The method of claim 17, [wherein the step of forming a gate structure] further [includes]comprising:

patterning the gate structure by selectively etching away portions of the insulating oxide, nitride and polysilicon layers to expose a portion of the substrate and form a peripheral edge around the gate structure; and

[wherein the reoxidizing step comprises] exposing the substrate to an oxidizing ambient during reoxidation to oxidize the exposed portion of the substrate.

21. (amended) The method of claim 20, wherein the [exposing step]reoxidation causes an uplift in a peripheral portion of the nitride layer.

22. (amended) The method of claim 20, wherein the [exposing step]reoxidation causes an indentation in the substrate near [a]the peripheral edge of the gate structure.

23. (amended) The method of claim 17, [wherein]further comprising:

prior to the reoxidizing step, forming source and drain regions in the substrate.

25. (amended) [The]A method [of claim 24]for fabricating a portion of a semiconductor device, comprising:

forming an oxide gate layer on a surface of a substrate;

[wherein the step of] forming a nitride layer [comprises]on the oxide gate layer by depositing [a]the nitride layer on the oxide gate layer;

forming a polysilicon layer on the nitride layer;

patterning the polysilicon and nitride layers to form a gate structure; and

reoxidizing the gate structure to form a layer of oxide over the gate structure and on sidewalls of the gate structure.

50. (amended) The integrated circuit device of claim 46, wherein the gate structure has a peripheral edge and further including an uplift in [the nitride layer occurring in] portions of the nitride layer proximate the peripheral edge of the gate structure, the uplift caused by reoxidation of the gate structure, wherein asperities are absent from the polysilicon layer.

51. (amended) The integrated circuit device of claim 46, wherein the substrate has a surface and further including an indentation in the surface of the substrate located proximate to the peripheral edge of the gate structure, the indentation resulting from reoxidation of the [integrated circuit device]gate structure.

52. (amended) The integrated circuit device of claim 46 further wherein the gate structure includes sidewall spacers located on each edge of the gate structure and lightly doped drain regions in the substrate [located in the substrate] below the sidewalls spacers.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting prosecution of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@novakov.com*.

Respectfully submitted,

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